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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,908	09/28/2004	Jhyy-Cheng Liou	JCLA6965-2	4264

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EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/509,908	LIOU ET AL.	
	Examiner	Art Unit	
	MARK PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-19 and 26-29* is/are rejected.

7)☒ Claim(s) *20-25 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

This Office Action is in response to the response filed on July 11, 2006.

Claim 22 is objected to for two reasons. First, "claim21" (line 1) should read "claim 21". Furthermore, "the two pairs of bank select transistors of the are arranged" (line 5) is unclear ("of the" should apparently be deleted). Correction is required.

Claims 23-25 depend on claim 22 and are thus similarly objected to.

Claims 17, 18 and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Prior Art Fig. 3 disclosure together with United States Patent 5,600,171 to Makihara et al. (Makihara).

As to independent claim 17, the Prior Art Fig. 3 disclosure discloses a NAND Mask ROM, comprising a plurality of word lines 302, a plurality of bit lines 320, and a plurality of memory cells arranged in rows and columns, wherein the memory cells include a plurality of first memory cells C1 acting like depletion MOS transistors of a first (n) channel conductivity by way of shorting interconnects 326, and a plurality of second memory cells C2 that have a second (p) channel conductivity and are enhanced MOS transistors; the memory cells in the same row are coupled to a word line, and the memory cells in the same column are coupled to a bit line; a constant number of continuous memory cells in the same column are grouped as a memory string 304, wherein a non-terminal memory cell shares a source and a drain with two adjacent memory cells in the memory string; and one terminal cell in the memory string is coupled to a bit line, and the other terminal memory cell is coupled to ground 306.

The difference between claim 17 and the Prior Art Fig. 3 disclosure is claim 17's plurality of first memory cells are actually depletion MOS transistors while the Prior Art Fig. 3

disclosure's plurality of first memory cells C1 act as depletion MOS transistors by way of shorting interconnects 326.

Makihara teaches using either actual depletion MOS transistors or transistors acting as depletion MOS transistors by way of shorting interconnects in a mask ROM device (see the entire patent, particularly the Figs. 9-11 disclosure, which discloses using actual depletion MOS transistors, and the Figs. 1-3 disclosure, which discloses using transistors acting as depletion MOS transistors by way of shorting interconnects 201-205).

It would have been obvious to one skilled in the art to form the Prior Art Fig. 3 disclosure's plurality of memory cells C1 as actual depletion MOS transistors rather than transistors acting as depletion MOS transistors by way of shorting interconnects because Makihara teaches using either actual depletion MOS transistors or transistors acting as depletion MOS transistors by way of shorting interconnects in a mask ROM device.

Claim 17 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over the Prior Art Fig. 3 disclosure together with Makihara.

As to dependent claim 18, the Prior Art Fig. 3 disclosure's memory cells comprise NMOS transistors, its second memory cells C2 comprise enhanced NMOS transistors that have P-type channels, and its first memory cells C1 as modified by Makihara's teaching would comprise actual depletion NMOS transistors that have N-type channels.

Claim 18 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over the Prior Art Fig. 3 disclosure together with Makihara.

As to dependent claim 26, the Prior Art Fig. 3 disclosure's memory string 304 is coupled to a bit line 320, and does not share the bit line with another memory string adjacent in the row dimension.

Claim 26 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over the Prior Art Fig. 3 disclosure together with Makihara.

As to dependent claim 27, one terminal memory cell in the Prior Art Fig. 3 disclosure's memory string 304 is coupled to a bit line 320 via one bank select transistor 308.

Claim 27 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over the Prior Art Fig. 3 disclosure together with Makihara.

As to dependent claim 28, a diffusion of the other terminal memory cell in the Prior Art Fig. 3 disclosure's memory string 304 is coupled to a ground line 306 via a contact.

Claim 28 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over the Prior Art Fig. 3 disclosure together with Makihara.

As to dependent claim 29, two of the Prior Art Fig. 3 disclosure's memory strings 304 (in adjacent columns) are separated by an isolation layer.

Claim 29 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over the Prior Art Fig. 3 disclosure together with Makihara.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Prior Art Fig. 3 disclosure together with United States Patent 5,600,171 to Makihara et al. (Makihara) and United States Patent 4,350,992 to Tubbs. Claim 19 depends on independent claim 17. The above rejection of independent claim 17 under 35 U.S.C. 103(a) as being unpatentable over the Prior Art Fig. 3 disclosure together with Makihara is incorporated by reference into this rejection

of dependent claim 19 under 35 U.S.C. 103(a) as being unpatentable over the Prior Art Fig. 3 disclosure together with Makihara and Tubbs.

As to dependent claim 19, the difference between it and the Prior Art Fig. 3/Makihara ROM is their memory cells comprise PMOS and NMOS transistors, respectively.

Tubbs teaches that ROM memory cells are conventionally formed of PMOS transistors or NMOS transistors (see the entire patent, including column 5, lines 26-27).

It would have been obvious to one skilled in the art to form the Prior Art Fig. 3/Makihara ROM's memory cells of PMOS transistors instead of NMOS transistors because Tubbs teaches that ROM memory cells are conventionally formed of PMOS transistors or NMOS transistors.

Claim 19 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over the Prior Art Fig. 3 disclosure together with Makihara together with Tubbs.

Claims 20-25 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not disclose or suggest the allowable NAND Mask ROM as a whole.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty
Mark V. Prenty
Primary Examiner